



LE910Cx Multi Technology Interface Board TLB

HW User Guide

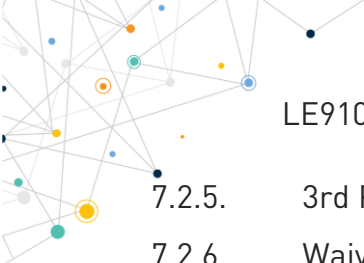
1VV0301508 Rev. 5 – 2022-02-02

APPLICABILITY TABLE

PRODUCTS
LE910C1-NA
LE910C1-AP
LE910C1-NS
LE910C4-NS
LE910C1-EU

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1. INTRODUCTION

1.1. Scope

The scope of this document is to describe the MultiTech Interface Board TLB which is part of the complete EVB Development Kit (Dev-Kit).

1.2. Audience

This document is intended for Telit customers, especially system integrators, about to implement their applications using the Telit LE910Cx module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report of documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com
- TS-ONEEDGE@telit.com

Alternatively, use:

<https://www.telit.com/contact-us>

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates the user feedback on our information.

1.4. Symbol Conventions



Danger: This information **MUST** be followed, or catastrophic equipment failure or personal injury may occur.



Warning: Alerts the user on important steps about the module integration.



Note/Tip: Provides advice and suggestions that may be useful when integrating the module.



Electro-static Discharge: Notifies the user to take proper grounding precautions before handling the product.

Table 1: Symbol Conventions

All dates are in ISO 8601 format, that is YYYY-MM-DD.

1.5. Related Documents

- LE910C1 HW User Guide, 1VV0301298
- Generic Evaluation Board Hardware User Guide, 1VV0301249

2. GENERAL DESCRIPTION

The MultiTech Interface Board TLB (aka MTB) is custom designed to interface the Telit module variant LE910Cx with the Telit Generic Evaluation Board (EVB) forming the complete LE910Cx Development Kit, allowing for great flexibility for integrating WIFI, The MultiTech Interface Board TLB (aka MTB) is custom designed to interface the Telit module variant LE910Cx with the Telit Generic Evaluation Board (EVB), forming the complete LE910Cx Development Kit, allowing for great flexibility in integrating WIFI, Bluetooth, and GPS technologies with the LE910Cx.

The MTB converts Telit module signals and functions into generic EVB signals and functions.

The following components are included in the MultiTech Interface Board TLB design:

- Module LE910Cx
- 3x M.2 mini card slots
- FPGA Programmable
- SMA RF connectors
- Board-to-Board connectors for connecting to the EVB main board
- Module-specific circuitry that is not part of the EVB's generic circuitry. and GPS technologies with the LE910Cx.


The MTB provides the mapping of Telit module signals and functions into the generic EVB signals and functions.

The MultiTech Interface Board TLB design includes the following components:

- LE910Cx module
- 3x M.2 type mini card slots
- Programmable FPGA
- RF SMA connectors
- Board to Board connectors for interfacing to EVB main board
- Module specific circuitry which is not part of the generic circuitry of the EVB.

Power supply and control interface for the cellular module is provided from the EVB via the B2B connectors.

To monitor the temperature, a thermistor is placed on the top GND plane, close to the module which should be representative for the module's backside temperature.



A programmable FPGA included in the MTB allows you to connect every functional modem pin to the relevant peripheral M.2 cards hence enabling the most flexible way to demonstrate interoperability between the LE910Cx module and peripheral accessories.

A typical example of this capability is in the case where 3x M.2 cards (WIFI module, GNSS module and BT module) are plugged into the M.2 slots while the FPGA is programmed to perform the correct signals mapping between the LE910Cx and the interfaces of each of the M.2 accessories.

2.1. MultiTech Interface Board TLB View

Figure 1 and Figure 2, show the MultiTech Interface Board TLB top and bottom views:



Figure 1: MultiTech Interface Board TLB - Top View



Figure 2: MultiTech Interface Board TLB - Bottom View

3. FPGA

The FPGA used in this board is a Lattice Semiconductor MACHX03 family device.

More information about this part can be found at:

<http://www.latticesemi.com/en/Products/FPGAandCPLD/MachX03>

The tools to write, compile, place, route, and program the FPGA can be downloaded from Lattice website.

The purpose of the FPGA in this board is to provide the maximum flexibility connecting different peripherals of the LE910Cx pins.

The board includes a rotary mode selector for selecting a pre-defined FPGA configuration for mapping the LE910Cx pins to the various peripherals.

For each mode, the signals from the module can be muxed to either or all of the M.2 slots or to the main board connectors on the bottom side (for interfacing to the EVB).

3.1. Programming the FPGA

This section details the steps needed to program/flash the FPGA.

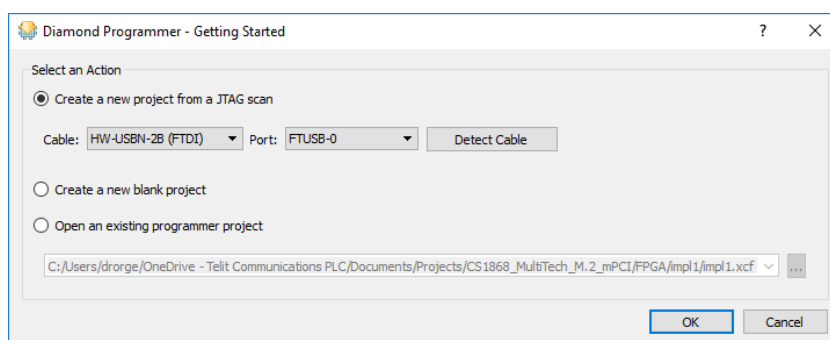
3.1.1. Prerequisites

1. The JEDEC file to be programmed. This is the file uploaded/flushed into the FPGA.
2. Installed Programming tool. This “Programmer and Deployment Tool” is available for free from the Lattice Semiconductor website:

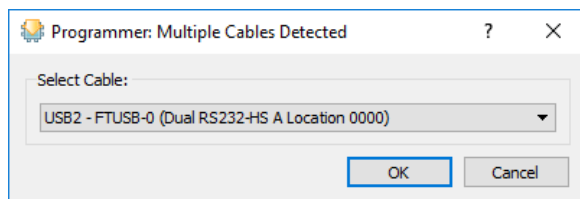
<http://www.latticesemi.com/Products/DesignSoftwareAndIP/ProgrammingAndConfigurationSw/Programmer>

To program the FPGA, follow these steps:

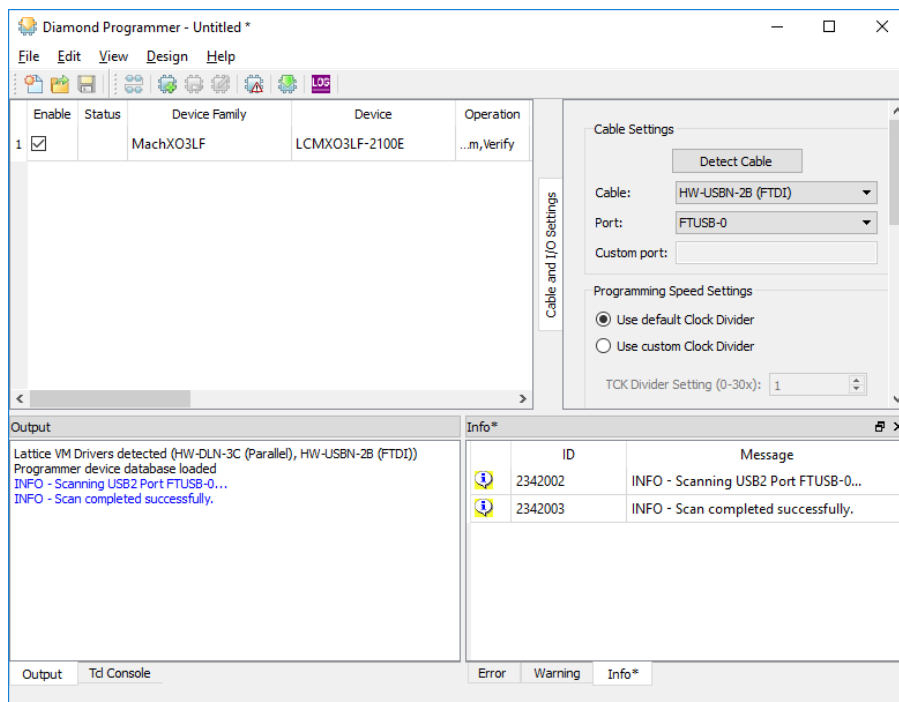
1. Power on the module (pressing the ON button on the EVB main board).
2. Launch the **Diamond Programmer** tool.
3. In the window that appears, click **Detect Cable**.




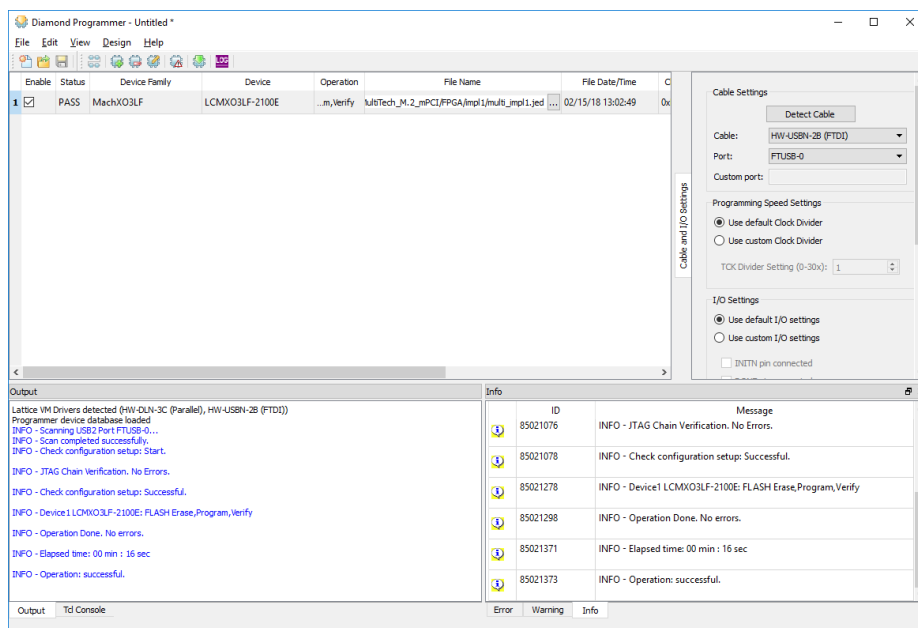
4. Select Cable and click **OK**.



5. The main program window will display scanning and searching for the FPGA component.



6. Click the line below **File name** and navigate to the JEDEC file location.. It is now recommended to save the programmer window setup.
7. To program the FPGA, either click the menu icon  or go to **Design** tab and select **Program**.
8. A successful program sequence should be acknowledged as shown below:



3.2. FPGA Mode Selection

As described previously, the board includes a rotary mode selection switch. The switch reference location is SW700. It is a rotary switch with 16 states decoded by the FPGA logic for the different modes needed.



Figure 3: FPGA Mode Selection Switch

The predefined modes currently supported by the FPGA are detailed below:

Mode Switch Selection	Functional Mode Description
0	Default
1	Slot1: SDIO, Main UART, WCI UART, DVI Slot2: SPI
2	Spare
3	Slot1: SDIO Slot2: Main UART, WCI UART Slot3: SPI
4	Spare

Mode Switch Selection	Functional Mode Description
5	Spare
6	Spare
7	Spare
8	Spare
9	Spare
10 (A)	LE910C1: Slot 1 HCI Bluetooth connection to EVB MAIN_UART (for testing only)
11 (B)	Spare
12 (C)	Spare
13 (D)	LE910 V2: SPI, I2C_GPIOs (10-SCL, 8-SDA) AT#I2CWR=8,10,30,4,19
14 (E)	LE910 V2: SPI to UART_AUX
15 (F)	LE910C1: WIFI SDIO SLOT1 (Normal EVB mode)

Table 2: FPGA Mode Selection



Note: Additional modes for supporting new bundling options may be released in the future.

For more information, please contact a Telit representative.

4. 120-PIN BOARD TO BOARD CONNECTORS

4.1. Board to Board Connector J1

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	GND	2	GND	3		4		5	GND	6	
7	USB_SS_RX_P	8	GND	9	I2C_SDA	10	TGPIO_06	11		12	
13	USB_SS_RX_M	14	GND	15	TGPIO_05	16	I2C_SCL	17		18	GND
19	GND	20	GND	21	VREG_MSME	22	VREG_MSME	23	GND	24	
25	USB_SS_TX_P	26	GND	27		28		29		30	
31	USB_SS_TX_M	32	GND	33		34	SPI_MOSI	35		36	GND
37	GND	38		39		40	TGPIO_04	41	GND	42	
43	SPI_CS	44	TGPIO_02	45	TGPIO_03	46	SPI_MISO	47		48	
49	VAUX/PWRMON	50	VAUX/PWRMON	51		52	SPI_CLK	53		54	
55	TGPIO_08	56	TGPIO_07	57	TGPIO_01	58	TGPIO_09	59		60	
61		62	TGPIO_10	63		64	TGPIO_20	65		66	
67	VMMC	68	VMMC	69	MMC_CD	70	MMC_DAT3	71		72	
73	MMC_DAT0	74	MMC_DAT2	75	MMC_CLK	76	MMC_DAT1	77		78	
79	GND	80	GND	81	C107/DSR	82	MMC_CMD	83		84	
85		86		87		88		89	TX_AUX	90	
91		92		93		94		95	RX_AUX	96	
97		98		99		100	WCI_TX	101	WCI_RX	102	
103	C125/RING	104	RFCLK2_QCA	105	WLAN_SLEEP_CLK	106	C105/RTS	107		108	
109	C104/RXD	110	C109/DCD	111	C103/TXD	112	C106/CTS	113	C108/DTR	114	
115		116		117		118		119		120	

Table 3: Board to Board Connector J1

4.2. Board to Board Connector J2

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	GPS_LNA_BIAS	2	GND	3	GPS_LNA_EN	4		5	GND	6	
7	GND	8	GND	9	GND	10	GND	11	GND	12	
13		14		15	GND	16		17		18	
19	GND	20	GND	21	GND	22	GND	23	GND	24	GND
25		26		27	GND	28		29		30	GND
31		32		33		34		35		36	
37	GND	38	GND	39		40		41	GND	42	GND
43		44	GND	45	GND	46	GND	47	GND	48	GND
49		50	GND	51	GND	52	ADC_IN3	53	ADC_IN2	54	ADC_IN1
55		56		57		58		59		60	
61	DVI_RX	62	DVI_TX	63	DVI_CLK	64	DVI_WA0	65	REF_CLK	66	GND
67	GND	68	GND	69	GND	70	GND	71	GND	72	
73	GND	74	GND	75	GND	76	GND	77	SIMVCC1	78	SIMVCC1
79	HSIC_STB	80	HSIC_DATA	81	SIMCLK1	82	SIMIN1	83	SIMIO1	84	SIMRST1
85		86	VRTC	87		88		89	SIMVCC2	90	SIMVCC2
91	USB_VBUS	92	USB_ID	93	SIMIN2	94	SIMIO2	95	SIMRST2	96	SIMCLK2
97	GND	98	GND	99		100		101		102	
103	USB_D+	104	GND	105		106		107		108	
109	USB_D-	110	GND	111		112		113		114	
115	GND	116	GND	117		118		119		120	

Table 4: Board to Board Connector J2

4.3. Board to Board Connector J3

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	VBATT	2	VBATT	3	VBATT	4	VBATT_PA	5	VBATT_PA	6	VBATT_PA
7	VBATT	8	VBATT	9	VBATT	10	VBATT_PA	11	VBATT_PA	12	VBATT_PA
13	VBATT	14	VBATT	15	VBATT	16	VBATT_PA	17	VBATT_PA	18	VBATT_PA
19		20		21		22	VBATT_PA	23	VBATT_PA	24	VBATT_PA
25		26		27		28		29		30	
31		32		33		34		35		36	
37		38		39		40		41		42	
43		44		45		46		47		48	
49		50		51		52		53		54	
55		56		57		58		59		60	
61		62		63		64		65		66	D8_THERM_ASTAR
67		68		69		70		71		72	
73		74		75		76		77		78	
79	GND	80	GND	81	GND	82	GND	83	GND	84	GND
85	GND	86	GND	87	GND	88	GND	89	GND	90	GND
91	RESET	92	ON_OFF	93	STAT_LED	94		95	SW_RDY	96	SHDN
97	GND	98	GND	99	GND	100	GND	101		102	
103	GPS_SYNC	104	GPS_RFPAON	105	GPS_CLK	106	GND	107		108	
109	GND	110	GND	111	GND	112	GND	113	JTAG_TDI	114	JTAG_PS_HOLD
115	JTAG_TMS	116	JTAG_TDO	117	JTAG_TRST	118	JTAG_TCK	119	JTAG_RTCK	120	JTAG_RESOUT

Table 5: Board to Board Connector J3

5. COMPONENT ASSEMBLY DIAGRAM

Searchable Layout:



CS1868A_Placement.
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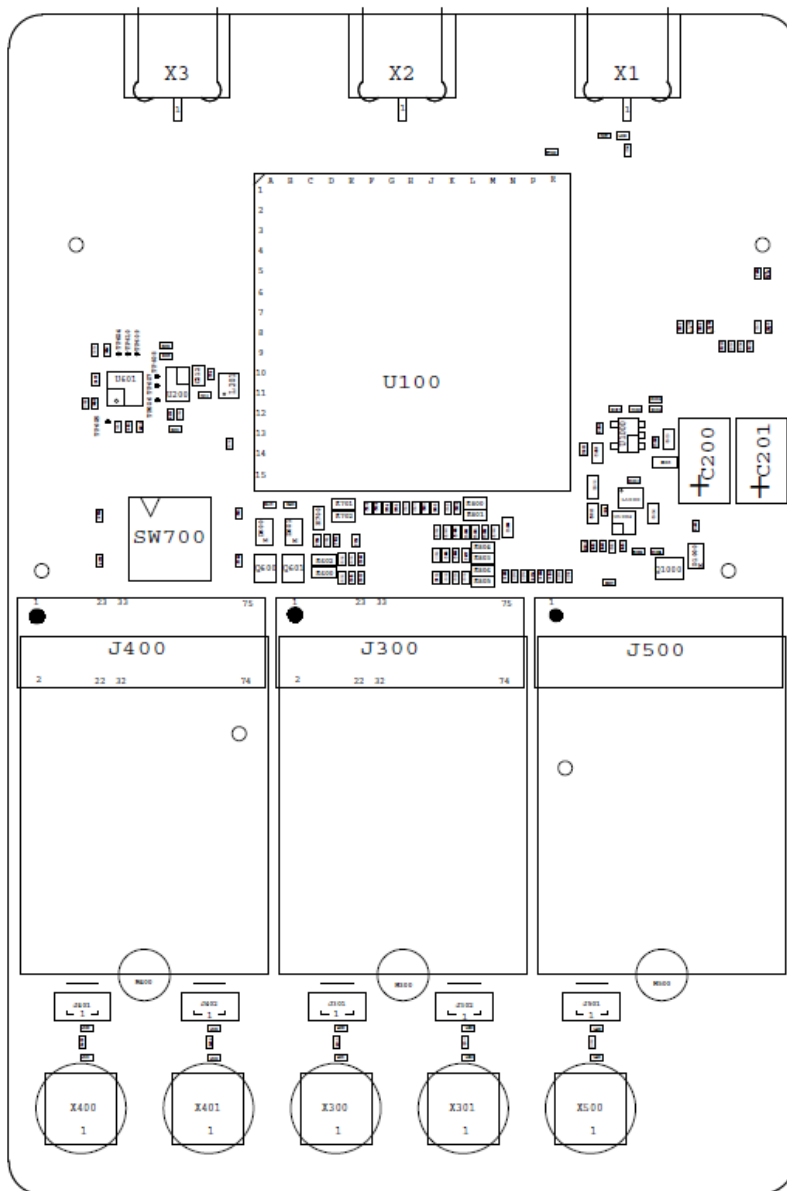


Figure 4: Component Diagram - Top View

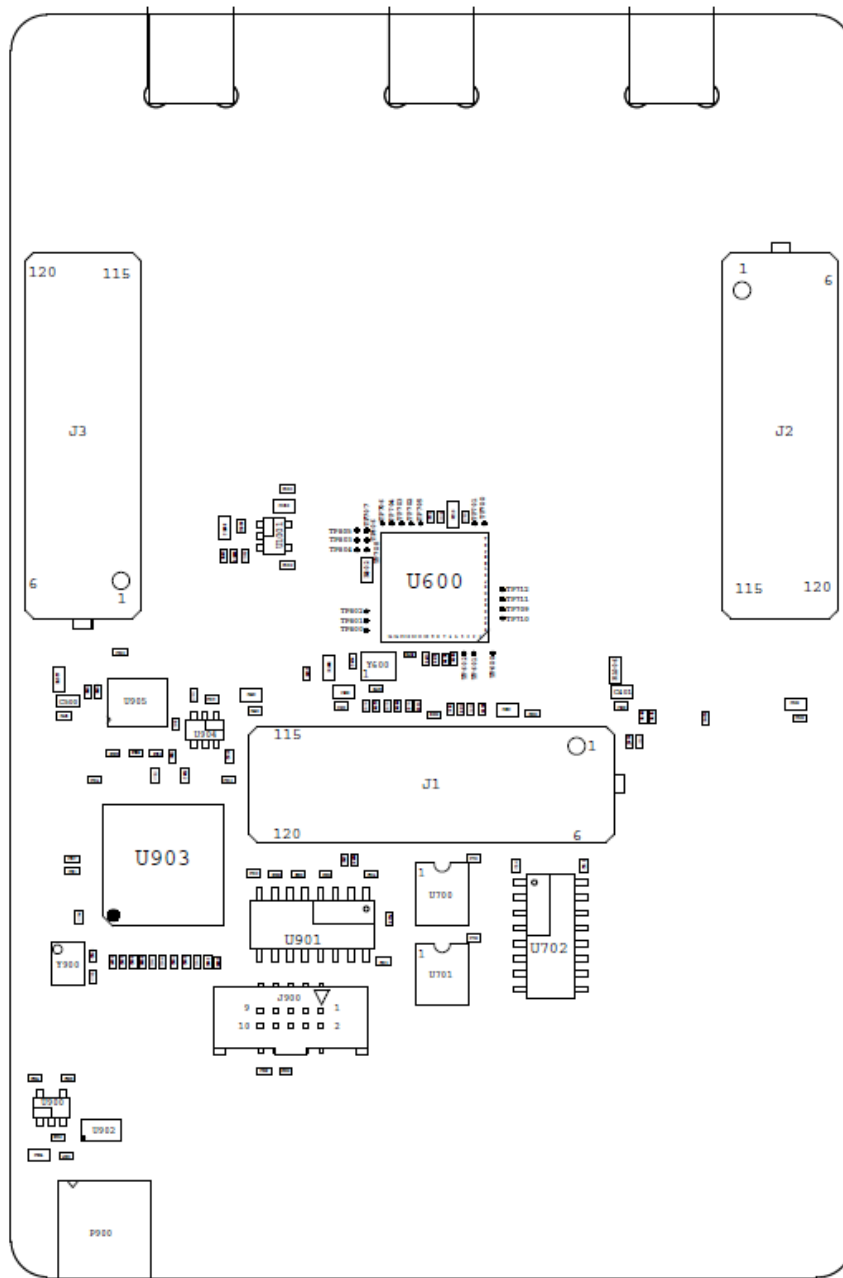


Figure 5: Component Diagram - Bottom View

6. SCHEMATICS



cs1868A-Schematics.
pdf

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Make sure the use of this product is allowed in your country and in the environment required. The use of this product may be dangerous and has to be avoided in areas where:

- it can interfere with other electronic devices, particularly in environments such as hospitals, airports, aircrafts, etc.
- there is a risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product. Therefore, the external components of the module, as well as any project or installation issue, have to be handled with care. Any interference may cause the risk of disturbing the GSM network or external devices or having an impact on the security system. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed carefully in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The equipment is intended to be installed in a restricted area location.

The equipment must be supplied by an external specific limited power source in compliance with the standard EN 62368-1:2014.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

https://ec.europa.eu/growth/sectors/electrical-engineering_en

8. GLOSSARY

EVB	Evaluation Board
IFBD	Interface Board
GPIO	General Purpose Input Output
SD	Secure Digital
UART	Universal Asynchronous Receiver Transmitter
UMTS	Universal Mobile Telecommunication System
USB	Universal Serial Bus
USIF	Universal Serial Interface
FPGA	Field Programmable Array

9. DOCUMENT HISTORY


Revision	Date	Changes
3	2022-02-02	Template updated
2	2019-03-08	Updated Table 1: FPGA Mode Selection.
1	2018-02-27	Initial Version

From Mod.0818 rev.3



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